IN THE CLAIMS:

WHAT IS CLAIMED IS:

1-25. (Cancelled).

26. (New) A memory device comprising:

a timing signal receive circuit to receive a first timing signal from a memory controller;

an input buffer to receive write data from the memory controller;

a data-in register coupled to the first timing signal receive circuit and the input buffer, the data-in register to clock receipt of the write data with the first timing signal;

output circuitry to transmit read data to the memory controller; and

a mode register to store a mode value indicative of memory device operation;

wherein when the mode value is set to a first value, the output circuitry to clock the read data with the first timing signal received from the memory controller, and

when the mode value is set to a second value, the output circuitry to clock the read data with a second timing signal.

27. (New) The memory device of claim 26, wherein the mode register is configured to store the mode value responsive to a command from the memory controller.

28. (New) The memory device of claim 26, the memory device coupled to a data bus, wherein the write data is received over the data bus, and the read data is transmitted over the data bus.

29. (New) The memory device of claim 26, the memory device coupled to a control and address bus, wherein the memory device is configured to receive over the control and address bus control and address signals from the memory controller.

30. (New) The memory device of claim 29, wherein the control and address signals are received in conjunction with the second timing signal, the second timing signal clocking receipt of the control and address signals.

31. (New) The memory device of claim 26, further comprising a multiplexor, the multiplexor coupled to the mode register, the multiplexor to provide the first timing signal to the output circuitry when the mode value is set to the first value and to provide the second timing signal to the output circuitry when the mode value is set to the second value.

32. (New) The memory device of claim 26, further comprising an output buffer, wherein when the mode value is set to the second value, the output buffer to drive the second timing signal as the timing signal for the read data being transmitted from the output circuitry.

33. (New) The memory device of claim 26, wherein when the mode value is set to the first value, the memory device receives the first timing signal continuously from the memory controller.

34. (New) The memory device of claim 26, wherein when the mode value is set to the second value, the memory device transmits the second timing signal to the memory controller.

35. (New) The memory device of claim 26, further comprising:

a data storage array to store the write data, the output circuitry coupled to the data storage array.

36. (New) A method of operating a memory device to store data in a memory system, comprising:

receiving a first timing signal from a memory controller;

receiving write data from the memory controller;

transmitting read data to the memory controller; and

clocking the read data corresponding to a stored mode value indicative of memory device operation, including:

when the mode value is set to a first value, clocking the write data with the first timing signal, and clocking the read data with the first timing signal, and

when the mode value is set to a second value, clocking the write data with the first timing signal, clocking the read data with a second timing signal.

37. (New) The method of claim 36, further comprising transmitting the second timing signal to the memory controller when the mode value is set to the second value.

38. (New) The method of claim 36, further comprising storing the mode value responsive to a command from the memory controller.

39. (New) The method of claim 36, further comprising receiving the write data over a data bus, and transmitting the read data over the data bus.

40. (New) The method of claim 36, further comprising receiving control and address signals from the memory controller over a control and address bus.

41. (New) The method of claim 40, further comprising clocking receipt of the control and address signals with the second timing signal.

42. (New) The method of claim 36, further comprising:

when the mode value is set to the second value, driving the second timing signal as the timing signal for the read data being transmitted to the memory controller.

43. (New) A memory device comprising:

input circuitry to receive a first timing signal and write data from a memory controller; and

output circuitry to output read data to the memory controller;

wherein in a first mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with the first timing signal, and

in a second mode of memory device operation, the input circuitry clocks the write data with the first timing signal and the output circuitry clocks the read data with a second timing signal.

44. (New) A memory device comprising:

input circuitry to receive a first timing signal and write data from a memory controller; and

output circuitry to output read data to the memory controller;

wherein in a first mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses the first timing signal as a phase reference while transmitting the read data, and

in a second mode of memory device operation, the input circuitry uses the first timing signal as a phase reference while receiving the write data and the output circuitry uses a second timing signal as a phase reference while transmitting the read data.

45. (New) A memory system, comprising

a memory controller, the memory controller to generate a first timing signal and to output first data;

a memory module comprising a first memory device having two modes of memory device operation, the first memory device to output second data;

an interconnect coupling the controller to the memory module, the first memory device to receive the first data over the interconnect and to transmit the second data over the interconnect; and

a timing signal bus coupling the controller to the memory module, the first memory device to receive the first timing signal over the timing signal bus;

wherein in a first mode of device operation, the first memory device clocks the first data and the second data with the first timing signal, and

in a second mode of device operation, the first memory device clocks the first data with the first timing signal and the second data with a second timing signal.

46. (New) The memory system of claim 45, the memory module further comprising:

a plurality of dynamic memory random access memory devices (DRAMs), the plurality of DRAMs including the first memory device.

47. (New) The memory system of claim 45, further comprising:

a control and address bus coupling the memory controller and the memory module.

48. (New) The memory system of claim 45, wherein when the first memory device operates in the first mode of device operation, the timing signal bus operates in a unidirectional mode, and wherein when the first memory device operates in the second mode of device operation, the timing signal bus operates in a bidirectional mode.

49. (New) The memory system of claim 48, wherein when the first memory device operates in the second mode of device operation, the memory device drives the second timing signal onto the timing signal bus.